The Method of Increasing the Immunity of Data Transmission in Communication Channels

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***Abstract* — The paper determines the benefits and feasibility of a method for additional gating of digital counts in "sliding window" mode followed by additional gating of its responses in both quadrature signal channels at once. The method of two-stage additional gating of analog-to-digital converter counts during I/Q demodulation of digital signals is analyzed.**

***Keywords*— amplitude-frequency response (AFC); analog-digital converter; digital signal processing; digital signal quadrature filter (DSQF); I/Q demodulation.**

I. Introduction

Modern analog-to-digital converters (ADCs) use high signal sampling frequencies, thereby imposing specific requirements on the speed of the digital segment of the data processing hardware. To simplify these requirements, thinning of the information flow is used. To ensure this process, the easiest way is to use only part of the ADC counts at the required interval, with the remaining ADC counts not used. This method has certain disadvantages, as it does not allow efficient use of signal energy, which leads to significant energy and information losses. Therefore, the actual task is to develop methods of additional ADC counts gating, which were devoid of the mentioned disadvantage and, moreover, have a reduced level of side lobes of the amplitude-frequency response (AFC) due to the use of preliminary analog or digital I/Q demodulation [1–6] of signal voltages.

II. The Aim of the Research

The paper aims to solve the problem of data loss and incorrect reproduction during data transmission in communication channels by increasing the noise immunity of the communication channel by constructing a tandem digital signal quadrature filter (DSQF) two-cascade circuit.

III. Materials and Methods

As you know, additional gating (decimation) of the analog-to-digital converter (ADC) counts [7, 8] allows for a reduction in the level of the side lobes of the amplitude-frequency characteristic of receiving channels of digital means of communication and provides quadrature (I/Q) demodulation signal voltage. In addition, it allows for simplifying the requirements for the construction of a digital path, which is especially important for making the development of digital antenna arrays cheaper [9–11].

With a single-channel circuit, ADC (Fig. 1) application of this version of the formation of quadrature component signals can be carried out in a tandem manner [6].

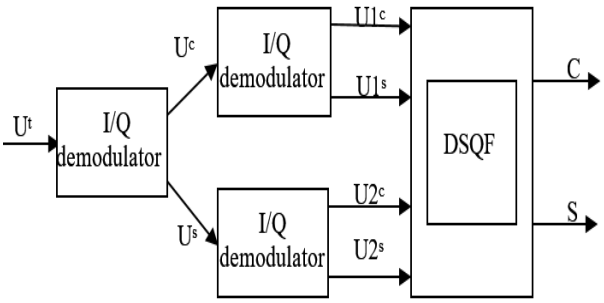

Fig. 1. DSQF tandem circuit with 2-stage I/Q demodulation

The processing of voltage readings in this DSQF cascade scheme (Fig.1) is described by expressions:

$$C=\sum_{y=0}^{y-1}(U1^{s}+U1^{c}), \quad (1)$$

$$S=\sum_{y=0}^{y-1}(U1^{s}-U1^{c}). \quad (2)$$

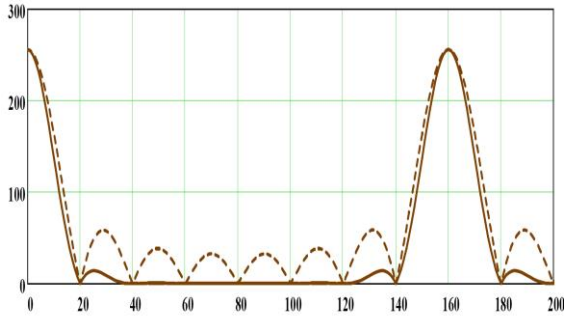

Fig. 2. AFC of a 2-cascade I/Q demodulation circuit

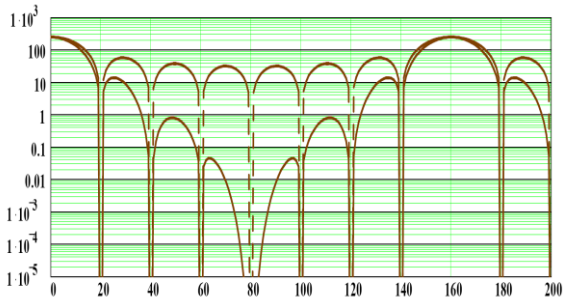

Fig. 3. AFC of a 2-cascade I/Q demodulation circuit in logarithmic scale

Fig. 2 and Fig. 3 illustrates the AFC of the tandem I/Q demodulation circuit from Fig. 1 (solid line), with the dashed line representing the AFC of the DSQF cascade of only one.

This variant of signal processing, as expected, does not allow for the elimination of the diffraction maximum in

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AFC (Fig. 2), resulting from the single-channel reception circuit, but reduces the level of side lobes due to double filtering in I/Q-demodulators.

An alternative option for performing additional gating of ADC counts (Fig. 4) consists of the distribution of operations of accumulation of counts of signal voltages obtained as a result of I/Q demodulation within two cascades, as shown in Fig. 4.

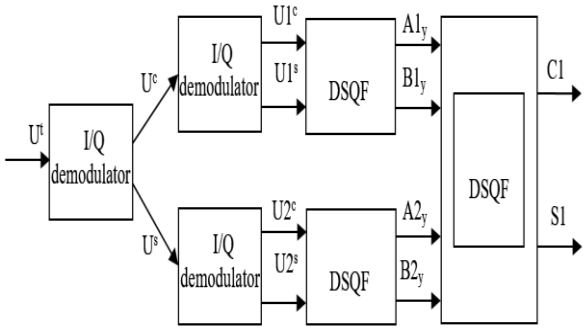

Fig. 4. Two-cascade implementation of counting decimation in the tandem DSQF circuit

In this case, the operation algorithm of the first cascade of the decimation of the output counts of I/Q-demodulators is implemented according to the expressions:

$$A1_y=\sum_{t=y*N}^{(y+1)N-1}\{U1^c\cos(\omega_0\tau t)+U1^s\sin(\omega_0\tau t)\}, \quad (3)$$

$$B1_y=\sum_{t=y*N}^{(y+1)N-1}\{U1^c\cos(\omega_0\tau t)-U1^s\sin(\omega_0\tau t)\}, \quad (4)$$

$$A2_y=\sum_{t=y*N}^{(y+1)N-1}\{U2^c\cos(\omega_0\tau t)+U2^s\sin(\omega_0\tau t)\}, \quad (5)$$

$$B2_y=\sum_{t=y*N}^{(y+1)N-1}\{U2^c\cos(\omega_0\tau t)-U2^s\sin(\omega_0\tau t)\}. \quad (6)$$

where ω_0 is the central radial frequency of the decimator AFC, τ is the sampling period of the ADC, and t is the sequence number of the counts of the output voltages of the I/Q demodulation results.

Whereas in the second decimation cascade, only the cross-summing of the signal counts accumulated in the strobes is performed according to the equations:

$$C1=A1_y+B2_y, \quad (7)$$

$$S1=B1_y-A2_y, \quad (8)$$

One limitation of the tandem circuit with multi-cascade I/Q demodulation (Fig. 4) is the non-uniformity of signal counts accumulation operations distribution between first and second decimation cascades. To eliminate this drawback, the improved version of tandem DSQF consists in modifying the processing of voltage counts in the last stage of the accumulator according to the expression:

$$C1=\sum_{y=0}^{y-1}(A1_y+B2_y), \quad (9)$$

$$S1=\sum_{y=0}^{y-1}(B1_y-A2_y). \quad (10)$$

at the same time, the calculation operations for other cascades remain unchanged (equation (3)–(6)).

The proposed variant of signal processing, presented in Fig. 5, allows the process of DSQF strobe count accumulation to be evenly distributed between two consecutive decimation cascades, which simplifies the bitness requirements for interfaces of inter-cascade data transmission, especially in multi-channel digital antenna arrays.

Similarly, to the multi-cascade inclusion of I/Q demodulators, it is possible to use multi-cascade combinations of I/Q demodulation and decimation circuits. Instead structure Fig. 1 a two-channel structural circuit fragment shown at the input of demodulators in Fig. 5 and Fig. 6 should be considered as a cascading element. Meanwhile, the initial formation of quadrature components should be carried out in an analog way.

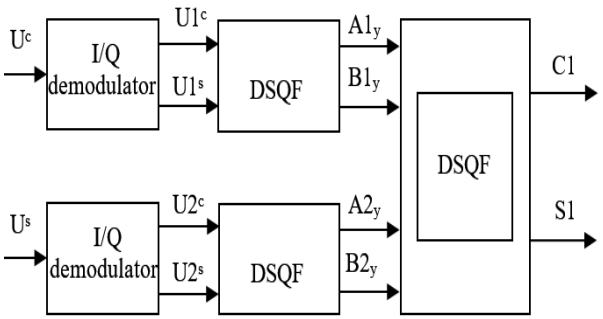

Fig. 5. Variant of a fragment of the tandem DSQF structural diagram with a uniform accumulation of counts between two decimation cascades

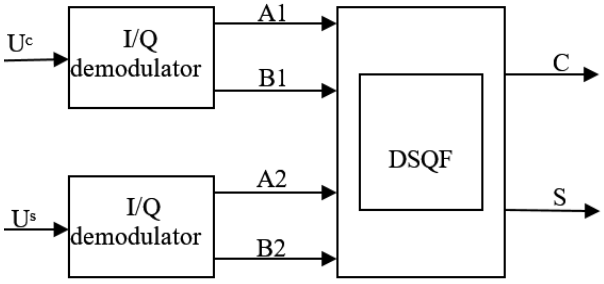

Fig. 6. Variant of the structural circuit of the tandem DSQF

Based on the cascading element in Fig. 6, in the case of the example in Fig. 7 shows a variant of two-stage tandem DSQF construction. This technical solution makes it possible to simplify the requirements for the speed of devices that implement the “sliding window” algorithm for the second cascade of I/Q demodulation, using low-order filters in it, while the application of I/Q demodulators of a larger dimension is transferred to the stage of processing strobe responses, where the speed data flow becomes much lower.

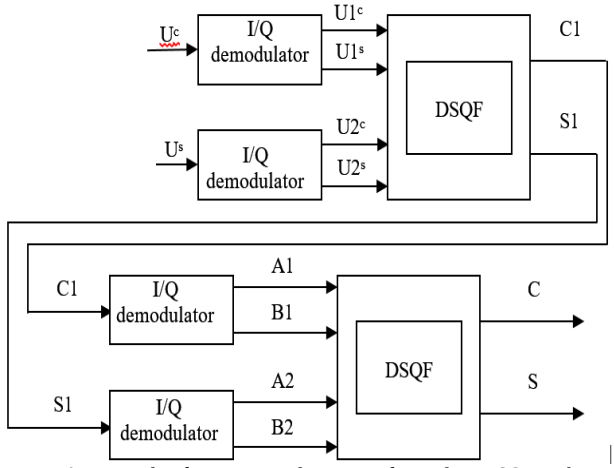

Fig. 7. An example of a two-cascade circuit of a tandem DSQF with a cascading element from Fig. 6.

In Fig. 8, Fig. 9, Fig. 10 and Fig. 11 illustrate the AFC of the signal processing procedure at 8- and 16-count strobing respectively, according to the tandem DSQF circuit (Fig. 7).

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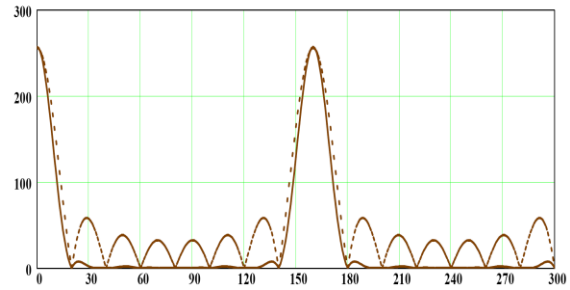

Fig. 8. Strobe 8 counts

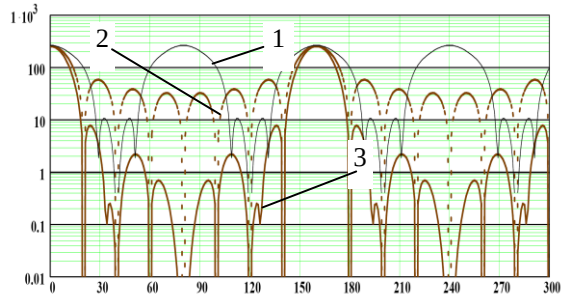

Fig. 9. Strobe 8 counts in a logarithmic scale

A feature of the specified tandem circuit (Fig. 7) there is a two-stage signal processing:

1st stage – application for a single-channel circuit of analog-to-digital conversion of voltage signals for weight processing of ADC counts in the "sliding window" mode according to the process of quadrature demodulation [1, 2]:

$$U_t^s = U_t - 11U_{t+2} + 15U_{t+4} - 5U_{t+6}\,, \quad (11)$$

$$U_t^c = 5U_{t+1} - 15U_{t+3} + 11U_{t+5} - U_{t+7}\,. \quad (12)$$

where t is the sequence number of the ADC counts, $U_t^{s(c)}$ is the quadrature voltage components;

2nd stage – use of the results of the indicated operation of weight processing of signals as an input array of quadrature counts for the two-channel operation of the decimation of ADC counts according to the equations:

$$W_y^c = \sum_{t=y*N}^{(y+1)N-1} \{U_t^c \cos(\omega_0 \tau t) + U_t^s \sin(\omega_0 \tau t)\}, \quad (13)$$

$$W_y^s = \sum_{t=y*N}^{(y+1)N-1} \{U_t^s \cos(\omega_0 \tau t) - U_t^c \sin(\omega_0 \tau t)\}. \quad (14)$$

where $U_t^{c(s)}$ is the quadrature components of the signal at the output operation of the digital quadrature demodulation ("sliding window"), y=0, Y-1 is the sequence number of the strobe, N is the number of ADC counts from which the decimation operation is performed, ω_0 is the central frequency of the decimator filter, τ is the ADC sampling period.

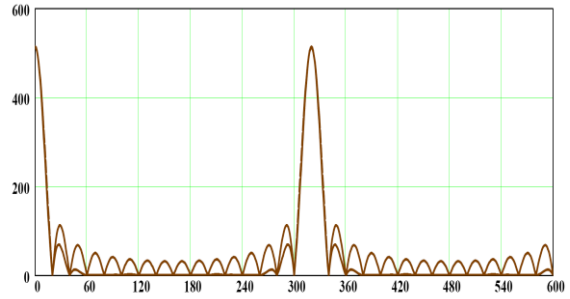

Fig. 10. Strobe 16 counts

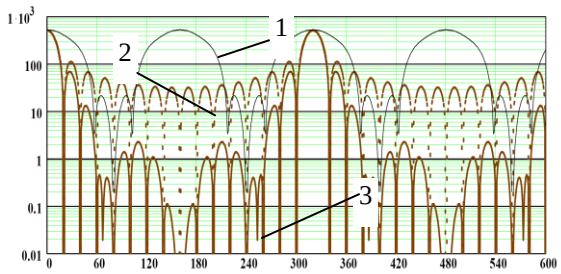

Fig. 11. Strobe 16 counts in a logarithmic scale

The disadvantage of the two-channel tandem DSQF construction options considered is the presence of large side lobes caused by the diffraction lobe of AFC I/Q-demodulators included in the first stage.

To eliminate this shortcoming, it is necessary to use cross-processing of counts of both quadrature [6]. One of the possible options for the implementation of such processing is reduced to the two-cascade inclusion of demodulators (Fig. 12), in which cross-processing is performed in the first stage of quadrature demodulation, and the second stage uses Fig. 5.

In Fig. 13, Fig. 14, Fig. 15 and Fig. 16 display the AFC of signal processing with 8- and 16-count strobing, respectively, according to the scheme of the improved tandem DSQF, presented in Fig. 12.

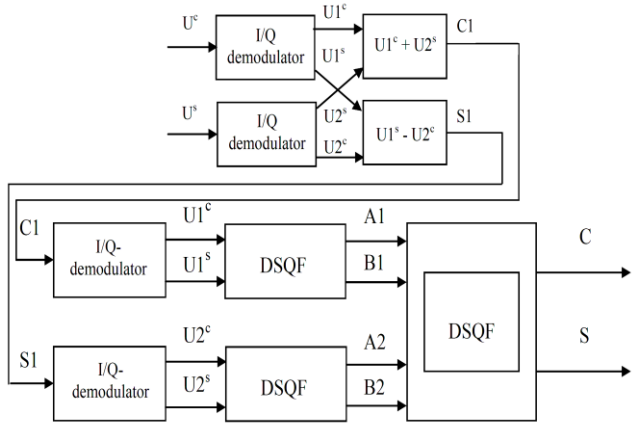

Fig. 12. Variation of the two-cascade circuit of the tandem DSQF with cross-processing of quadrature

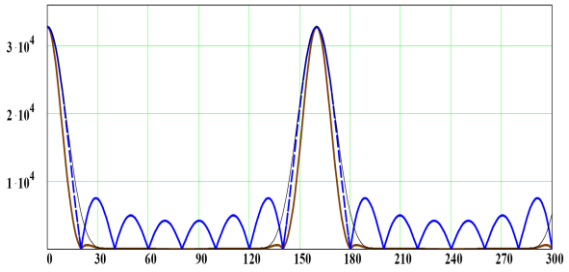

Fig. 13. Strobe 8 counts

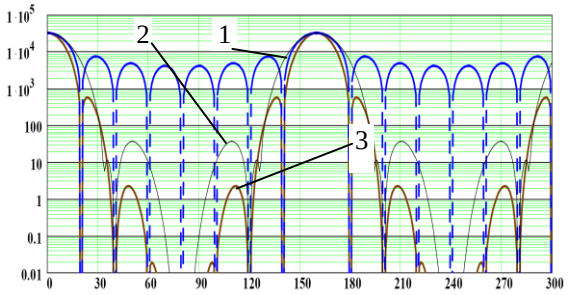

Fig. 14. Strobe 8 counts in a logarithmic scale

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In Fig. 14 and Fig. 16, line 1 corresponds to the AFC of the DSQF additional strobing filter [7, 8], line 2 is the AFC of DSQF in Fig. 7, and line 3 of the improved tandem scheme of Fig. 12 in total.

Thus, based on the results of mathematical modeling it was confirmed that the application of two-cascade I/Q-demodulation circuit as part of DSQF (Fig. 12) allows for achieving deeper suppression of DSQF side lobes. This has a positive effect on improving the noise immunity of receivers in digital communications under conditions of out-of-band interference [12], as well as improving the electromagnetic compatibility of radio engineering systems [13]. The corresponding benefit significantly depends on the dimensionality of the quadrature demodulators (filter order), the selected demodulator weighting factors, as well as the strobe lengths in the additional strobe filters for the sequences of digital counts.

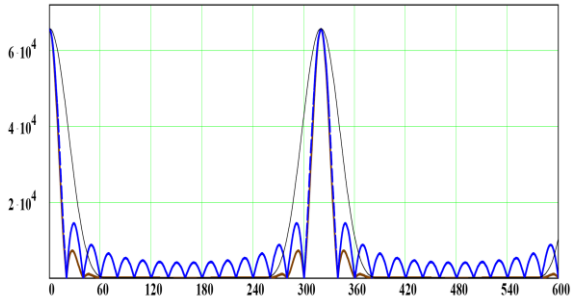

Fig. 15. Strobe 16 counts

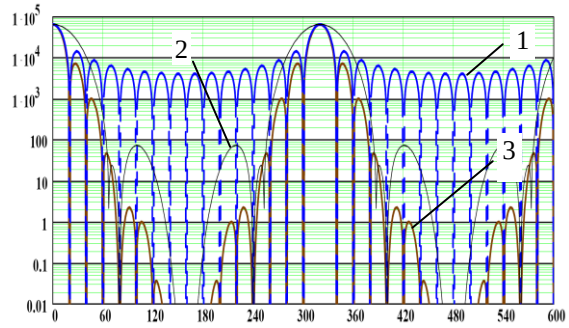

Fig. 16. Strobe 16 counts in a logarithmic scale

IV. Conclusion

According to the research findings, it should be concluded that the issue of improving the quality of quadrature signal demodulation is quite relevant for the further development of digital communications. Its effective solution is possible on the basis of a combination of technologies of digital quadrature demodulation of signals and additional strobing of their digital counts. At the same time, the electromagnetic compatibility and noise immunity of the corresponding radio facilities will be improved.

Further scientific research should be focused on finding ways to replace tandem digital quadrature signal demodulation circuits with additional strobing of digital counts with equivalent single-cascade circuits. This will simplify the corresponding hardware implementation based on FPGAs or ASICs [14–17] and will make it possible to reduce the cost of communication systems realizing the Massive MIMO technology [18, 19], as well as other radio engineering systems using multi-channel digital antenna arrays [9–11].

References

[1] *Swedish patent* No. 501604 (C2). IPC G11C27/02, H03D1/22. Method and apparatus for sampling of electrical signals.// Arvidsson Erik Ragnar. – Appl. number SE19930002627. - Priority date: 1993-08-13. – Publ. date: 1995-03-27.

[2] J.E. Eklund and R. Arvidsson, "A multiple sampling, single A/D conversion technique for I/Q demodulation in CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1987–1994, *1996.*

[3] C. Ziomek and P. Corredoura, "Digital I/Q demodulator", *Proceedings Particle Accelerator Conference*, vol. 4, 2002, pp. 2663-2665.

[4] D. Bernal, P. Closas, and J. A. Fernández-Rubio, "Digital I&Q demodulation in array processing: Theory and implementation," *16th European Signal Processing Conference*, 2008, Accessed: 17-Apr-2020.

[5] V. Slyusar and P. Serdiuk, "Synthesis method of procedure for odd-order I/Q demodulation based on replacing multistage with equivalent single-stage demodulation schemes," *Radioelectronics and Communications Systems*, vol. 63, no. 5, pp. 273–280, 2020.

[6] V. Slyusar and E. Zhivilo, "The synthesys of equivalence digital filters for tandem decimation on base I/Q-demodulation," *4th International Scientific-Practical Conference Problems of Infocommunications Science and Technology*, pp. 449-451, 2017.

[7] V. Slyusar, "Synthesis of algorithms for measurement of range to M sources with the use of additional gating of the ADC readings," *Radioelectronics and Communications Systems*, 1996, vol. 39, no. 5, pp. 36–40.

[8] I. Sliusar, S. Voloshko, V. Smolyar, and V. Slyusar, "Next generation optical access based on N-OFDM with decimation," *3rd International Scientific-Practical Conference Problems of Infocommunications Science and Technology*, pp. 192–194, 2016.

[9] V. I. Slyusar, "Origins of the Digital Antenna Array theory," *2017 XI International Conference on Antenna Theory and Techniques (ICATT)*, pp. 199–201, 2017.

[10] Yue Tang, Tian Mao, Bing Jiang, "Design and Experiment of Multi-resolution Composite Digital Array Antenna," *Journal of Radars*, vol. 5, no. 3, pp. 265-270, 2016.

[11] A. A. Vasin, L. I. Ponomarev, and O. P. Cheremisin, "High-accuracy direction finding of arbitrarily correlated multipath signals with the use of digital antenna arrays," *Journal of Communications Technology and Electronics*, vol. 60, no. 12, pp. 1311–1321, 2015.

[12] C. J. Hegarty, D. Bobyn, J. Grabowski, and A. J. Van Dierendonck, "An overview of the effects of out-of-band interference on GNSS receivers," *NAVIGATION*, vol. 67, no. 1, pp. 143–161, 2020.

[13] S. Cai, Y. Li, H. Zhu, X. Wu, and D. Su, "A novel electromagnetic compatibility evaluation method for receivers working under pulsed signal interference environment," *Applied Sciences*, vol. 11, no. 20, p. 9454, 2021.

[14] M. Mfana and A. N. Hasan, "Soft-core architecture for odd/even order sampling I/Q demodulator with dual-portblock memory considerations," *Preprints 2019*, 2019090014.

[15] J. Mitra and T. K. Nayak, "An FPGA-Based Phase Measurement System," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 1, pp. 133-142, Jan. 2018.

[16] L. Syllaios, "Hybrid and DS programmable phase/frequency detector for IoT chipsets," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 2018-May, 2018.

[17] P. I. Puzyrev, K. V. Semenov, and S. A. Zavyalov, "Spurious-free dynamic range of Cordic based digital quadrature demodulator," *2018 19th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM)*, vol. 2018-May, pp. 167–171, 2018.

[18] L. N. Ribeiro, S. Schwarz, M. Rupp, A. L. de Almeida, and J. C. Mota, "A low-complexity equalizer for massive MIMO systems based on array separability," 2017 25th European Signal Processing Conference (EUSIPCO), pp. 2522–2526, Aug. 2017

[19] C. D'Andrea, S. Buzzi, and M. Lops, "Communications and radar coexistence in the massive MIMO regime: Uplink Analysis," *IEEE Transactions on Wireless Communications*, vol. 19, no. 1, pp. 19–33, 2020.

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